

FORM PT01449  
(REV. 8-83)U. S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE

ATTY. DOCKET NO.

HARI.006USG

SERIAL NO.

08/931,133

APPLICANT

Eliyahou Harari et al.

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September 16, 1997

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2785

INFORMATION DISCLOSURE STATEMENT  
(Use several sheets if necessary)

## U. S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER									DATE	NAME	CLASS	SUB CLASS	FILING DATE
	A1	4	0	9	3	9	8	5			1978	Das			
	A2	4	2	7	9	0	2	4			1981	Schrenk			
	A3	4	6	1	6	3	1	1			1986	Sato			
	A4	4	7	1	8	0	4	1			1988	Baglee et al.			
	A5	4	7	8	5	4	2	5			1988	Lavelle			
	A6	4	8	0	0	5	2	0			1989	Iijima			
	A7	4	8	8	7	2	3	4			1989	Iijima			
	A8	4	9	4	9	2	4	0			1990	Iijima			
	A9	5	0	5	3	9	9	0			1991	Kreifels et al.			
	A10	5	0	7	0	4	7	4			1991	Tuma et al.			
	A11	5	0	9	5	3	4	4			1992	Harari			

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER									DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
	B1	58	-	2	1	5	7	9	4		1983	Japan			Yes
	B2	58	-	2	1	5	7	9	5		1983	Japan			Yes
	B3	59	-	1	6	2	6	9	5		1984	Japan			Yes
	B4	60	-	2	1	2	9	0	0		1985	Japan			Yes
	B5	62	-	2	8	3	4	9	6		1987	Japan			Yes

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

	C1	Lucero et al., "A 16 kbit Smart 5 V-only EEPROM with Redundancy," <i>IEEE Journal of Solid-State Circuits</i> , vol. SC-18, no. 5, pps. 539-543 (October 1983)
	C2	Torelli et al., "An improved method for programming a word-erasable EEPROM," <i>Alta Frequenza</i> , vol. 52, no. 6, pps. 487-494 (Nov.-Dec. 1983)
	C3	Data Sheet: "27F256 256K(32K x 8) CMOS Flash Memory," <i>Intel Corporation</i> , pps. 1-24 (May 1988)

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*EXAMINER INITIAL		DOCUMENT NUMBER								DATE	NAME	CLASS	SUB CLASS	FILING DATE
	A12	5	2	2	6	1	6	8		1993	Kobayashi et al.			
	A13	4	2	1	0	9	5	9		1980	Wozniak			
	A14	4	6	4	2	7	5	9		1987	Foster			
	A15	4	4	5	6	9	7	1		1984	Fukuda et al.			
	A16	4	2	9	5	2	0	5		1981	Kunstadt			
	A17	4	6	1	7	6	2	4		1986	Goodman			
	A18	4	3	5	4	2	5	3		1982	Naden			
	A19	4	4	2	2	1	6	1		1983	Kressel et al.			
	A20	4	4	5	0	5	5	9		1984	Bond et al.			
	A21	4	6	5	4	8	4	7		1987	Dutton			
	A22	4	7	3	3	3	9	4		1988	Burkhard			

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER								DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
	B6	60	-	0	7	6	0	9	7	1985	Japan			Abstr
	B7	59	-	4	5	6	9	5		1984	Japan			Abstr
	B8	61	-	9	6	5	9	8		1986	Japan			Abstr
	B9	62	-	2	8	3	4	9	7	1987	Japan			Abstr
	B10	63	-	1	8	3	7	0	0	1988	Japan			Abstr

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

	C4	Preliminary Data Sheet, "48F512 512K Flash EEPROM," SEEQ Technology, Incorporated, pps. 2-1 thru 2-12 (October 1988)
	C5	Advanced Data Sheet, "48F010 1024K Flash EEPROM," SEEQ Technology, Incorporated, pps. 2-13 thru 2-24 (October 1988)
	C6	Lai, Robert S., Writing MS-DOS Device Drivers, The Waite Group, Inc., September 1987, pp. i-xi and 235-319

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A23	4	8	9	6	2	6	2		1990	Wayama et al.			
A24	4	9	4	5	5	3	5		1990	Hosotani et al.			
A25	4	3	8	0	0	6	6		1983	Spencer et al.			
A26	4	4	6	3	4	5	0		1984	Haeusele			
A27	4	3	5	5	3	7	6		1982	Gould			
A28	3	6	3	3	1	7	5		1972	Harper			
A29	4	4	9	8	1	4	6		1985	Martinez			
A30	4	9	2	4	3	3	1		1990	Robinson et al.			
A31	4	4	7	9	2	1	4		1984	Ryan			
A32	4	9	5	3	1	2	2		1990	Williams			
A33	4	9	2	0	5	1	8		1990	Nakamura et al.			

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER								DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
B11	0	0	8	6	8	8	6		1983	European Patent Appln.				
B12	2	1	3	6	9	9	2	A	1984	UK Patent Appln.				
B13	0	2	4	3	5	0	3	B1	1987	European Patent Appln.				
B14	0	3	0	0	2	6	4	B1	1989	European Patent Appln.				
B15	0	5	5	7	7	2	3		1987	AU Patent Abridgement				

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

C7	Miller, "Semidisk Disk Emulator," Interface Age, p. 102, November, 1982												
C8	Clewitt, "Bubble Memories as a Floppy Disk Replacement," 1978 MIDCON Technical Papers, vol. 2, pp. 1-7, Dec. 1978												
C9	Hancock, "Architecting a CCD Replacement for the IBM 2305 Fixed Head Disk Drive," Digest of Papers, Eighteenth IEEE Computer Society International Conference, pp. 182-184, 1979												
C10	Wilson, "1-Mbit flash memories seek their role in system design," Computer Design, vol. 28, no. 5, pps. 30-32 (March 1989)												

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		A	3	4	9	3	0	7	5						
	A34	4	4	9	3	0	7	5		1985	Anderson et al.				
	A35	4	7	9	6	2	3	3		1989	Awaya et al.				
	A36	4	9	1	4	5	2	9		1990	Bonke				
	A37	4	0	5	1	3	5	4		1977	Choate				
	A38	5	1	6	3	0	2	1		1992	Mehrotra et al.				
	A39	4	5	1	4	8	3	0		1985	Hagiwara et al.				
	A40	4	7	9	4	5	6	8		1988	Lim et al.				
	A41	4	6	1	2	6	4	0		1986	Mehrotra et al.				
	A42	4	5	2	7	2	5	1		1985	Nibby, Jr., et al.				
	A43	4	7	4	6	9	9	8		1988	Robinson et al.				
	A44	4	9	4	2	5	5	6		1990	Sasaki et al.				
	A45	4	4	0	5	9	5	2		1983	Slakmon				
	A46	4	6	7	2	2	4	0		1987	Smith et al.				
	A47	4	2	5	0	5	7	0		1981	Tsang et al.				
	A48	4	6	0	1	0	3	1		1986	Walker et al.				
	A49	4	2	8	1	3	9	8		1981	McKenny et al.				
	A50	4	6	1	7	6	5	1		1986	Ip, et al.				

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER								DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)	
		B	1	6	W	O	8	4	0						
	B16	W	O	8	4	0	0	6	2	1984	PCT W.I.P.O.				
	B17	A	0	1	0	5	4	5	4	3	1989	Japanese Patent Abstr.			Yes
	B18	A	6	0	1	7	8	5	6	4	1986	Japanese Patent Abstr.			Yes

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

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## U. S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER							DATE	NAME		CLASS	SUB CLASS	FILING DATE
	A51	4	4	4	9	2	0	5		1984	Hoffman			
	A52	4	8	0	5	1	0	9		1989	Kroll et al.			
	A53	4	8	2	1	2	4	0		1989	Nakamura et al.			
	A54	4	8	8	2	6	4	2		1989	Tayler et al.			
	A55	4	9	2	0	4	7	8		1990	Furuya et al.			
	A56	4	9	3	3	9	0	6		1990	Terada et al.			
	A57	5	1	3	6	5	4	6		1992	Fukuda et al			
	A58	5	0	5	1	8	8	7		1991	Berger et al.			
	A59	4	9	1	6	6	0	5		1990	Beardsley et al.			
	A60	4	4	6	6	0	5	9		1984	Bastian et al.			
	A61	5	0	4	3	9	4	0		1991	Harari			
	A62	5	1	7	2	3	3	8		1992	Mehrotra et al.			
	A63	5	6	7	1	2	2	9		1997	Harari et al.			
	A64	5	2	9	7	1	4	8		1994	Harari et al.			
	A65	5	3	5	9	5	6	9		1994	Fujita et al.			
	A66	5	4	3	0	8	5	9		1995	Norman et al.			
	A67	5	4	8	8	7	1	1		1996	Hewitt et al.			
	A68	5	6	0	6	5	3	2		1997	Lambrache et al.			
	A69	5	5	4	6	3	5	1		1996	Tanaka et al.			

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

	C11	Bleiker et al., "A Four-State EEPROM Using Floating-Gate Memory Cells," <u>IEEE Journal of Solid-State Circuits</u> , SC-22 (1987) June, No. 3, New York, NY, USA
	C12	Intel Corporation, 27F256, 256K (32K x 8) CMOS FLASH MEMORY, May 1988, pp. 1-21

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INFORMATION DISCLOSURE STATEMENT <i>(Use several sheets if necessary)</i>		APPLICANT Eliyahou Harari et al.	
		FILED September 16, 1997	GROUP 2785

**U. S. PATENT DOCUMENTS**

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
	C13	Krick, "Three-State MNOS FET Memory Array," <u>IBM Technical Disclosure Bulletin</u> , Vol. 18, No. 12, May 1976, pp. 4192-4193					
	C14	Alberts C.S. et al., "Multi-Bit Storage FET EAROM Cell," <u>IBM Technical Disclosure Bulletin</u> , Vol. 24, No. 74, December 1981, pp 3311-3314					
	C15	Horiguchi et al., "An Experimental Large-Capacity Semiconductor File Memory Using 16-Levels Cell Storage," <u>IEEE Journal of Solid-State Circuits</u> , Vol. 23, No. 1, February 1988, pp.27-33					
	C16	Furuyama, et al., "An Experimental 2-Bit/Cell Storage Dram for Macro Cell or Memory-on-logic Application," <u>1988 IEEE</u> , pp. 4.4.1 to 4.4.4					
	C17	Stark, "Two Bits Per Cell ROM," <u>1981 IEEE Catalog No. 81-CH1626-1</u> , pp. 201-212					

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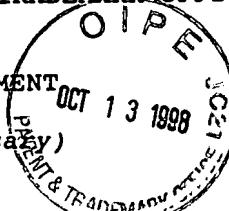
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PMC	A1	4	2	7	9	0	2	4	7	1981	Schrenk					
	A2	4	6	1	6	3	1	1	10	1986	Sato					
	A3	4	7	1	8	0	4	1	11	1988	Baglee et al.					
	A4	4	7	8	5	4	2	5	11	1988	Lavelle					
	A5	4	8	0	0	5	2	0	11	1989	Iijima					
	A6	4	8	8	7	2	3	4	12	1989	Iijima					
	A7	4	9	4	9	2	4	0	13	1990	Iijima					
	A8	5	0	5	3	9	9	0	10	1991	Kreifels et al.					
	A9	5	0	7	0	4	7	4	12	1991	Tuma et al.					
✓	A11	5	0	9	5	3	4	4	13	1992	Harari					

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PMC	B1	58	-	2	1	5	7	9	4	12	1983	Japan				Yes
	B2	58	-	2	1	5	7	9	5	12	1983	Japan				Yes
	B3	59	-	1	6	2	6	9	5	9	1984	Japan				Yes
	B4	60	-	2	1	2	9	0	0	10	1985	Japan				Yes
✓	B5	62	-	2	8	3	4	9	6	12	1987	Japan				Yes

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

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PMC	C2	Torelli et al., "An improved method for programming a word-erasable EEPROM," <i>Alta Frequenza</i> , vol. 52, no. 6, pps. 487-494 (Nov.-Dec. 1983)
PMC	C3	Data Sheet: "27F256 256K(32K x 8) CMOS Flash Memory," Intel Corporation, pps. 1-24 (May 1988)

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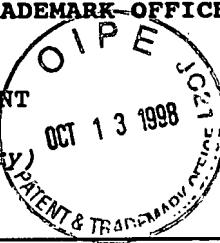
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Qmc		A12	5	2	2	6	1	6	8	7/1993	Kobayashi et al.			
		A13	4	2	1	0	9	5	9	7/1980	Wozniak			
		A14	4	6	4	2	7	5	9	2/1987	Foster			
		A15	4	4	5	6	9	7	1	6/1984	Fukuda et al.			
		A16	4	2	9	5	2	0	5	10/1981	Kunstadt			
		A17	4	6	1	7	6	2	4	10/1986	Goodman			
		A18	4	3	5	4	2	5	3	10/1982	Naden			
		A19	4	4	2	2	1	6	1	12/1983	Kressel et al.			
		A20	4	4	5	0	5	5	9	5/1984	Bond et al.			
		A21	4	6	5	4	8	4	7	3/1987	Dutton			
Qmc		A22	4	7	3	3	3	9	4	3/1988	Burkhard			

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Qmc		B6	60	-	0	7	6	0	9	7/1985	Japan			Abstr	
		B7	59	-	4	5	6	9	5	3/1984	Japan			Abstr	
		B8	61	-	9	6	5	9	8	5/1986	Japan			Abstr	
		B9	62	-	2	8	3	4	9	7/1987	Japan			Abstr	
		B10	63	-	1	8	3	7	0	0	7/1988	Japan			Abstr

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Qmc	C5	Advanced Data Sheet, "48F010 1024K Flash EEPROM," SEEQ Technology, Incorporated, pps. 2-13 thru 2-24 (October 1988)
Qmc	C6	Lai, Robert S., Writing MS-DOS Device Drivers, The Waite Group, Inc., September 1987, pp. i-xi and 235-319

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PMC	A23	4	8	9	6	2	6	2		1/1990	Wayama et al.	1	1		
	A24	4	9	4	5	5	3	5		7/1990	Hosotani et al.				
	A25	4	3	8	0	0	6	6		4/1983	Spencer et al.				
	A26	4	4	6	3	4	5	0		7/1984	Haeusele				
	A27	4	3	5	5	3	7	6		10/1982	Gould				
	A28	3	6	3	3	1	7	5		1/1972	Harper				
	A29	4	4	9	8	1	4	6		2/1985	Martinez				
	A30	4	9	2	4	3	3	1		5/1990	Robinson et al.				
	A31	4	4	7	9	2	1	4		10/1984	Ryan				
	A32	4	9	5	3	1	2	2		8/1990	Williams				
↓	A33	4	9	2	0	5	1	8		1/1990	Nakamura et al.				

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	B12	2	1	3	6	9	9	2	A	9/1984	UK Patent Appln.			
	B13	0	2	4	3	5	0	3	B1	7/1987	European Patent Appln.			
	B14	0	3	0	0	2	6	4	B1	10/1989	European Patent Appln.			
↓	B15	0	5	5	7	7	2	3		1/1987	AU Patent Abridgement			

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PMC	C7	Miller, "Semidisk Disk Emulator," <i>Interface Age</i> , p. 102, November, 1982
PMC	C8	Clewitt, "Bubble Memories as a Floppy Disk Replacement," <i>1978 MIDCON Technical Papers</i> , vol. 2, pp. 1-7, Dec. 1978
PMC	C9	Hancock, "Architecting a CCD Replacement for the IBM 2305 Fixed Head Disk Drive," <i>Digest of Papers, Eighteenth IEEE Computer Society International Conference</i> , pp. 182-184, 1979
PMC	C10	Wilson, "1-Mbit flash memories seek their role in system design," <i>Computer Design</i> , vol. 28, no. 5, pps. 30-32 (March 1989)

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*EXAMINER INITIAL		DOCUMENT NUMBER									DATE	NAME	CLASS	SUB CLASS	FILING DATE
Pme		A34	4	4	9	3	0	7	5		1/1985	Anderson et al.			
		A35	4	7	9	6	2	3	3		1/1989	Awaya et al.			
		A36	4	9	1	4	5	2	9		4/1990	Bonke			
		A37	4	0	5	1	3	5	4		9/1977	Choate			
		A38	5	1	6	3	0	2	1		11/1992	Mehrotra et al.			
		A39	4	5	1	4	8	3	0		4/1985	Hagiwara et al.			
		A40	4	7	9	4	5	6	8		12/1988	Lim et al.			
		A41	4	6	1	2	6	4	0		9/1986	Mehrotra et al.			
		A42	4	5	2	7	2	5	1		7/1985	Nibby, Jr., et al.			
		A43	4	7	4	6	9	9	8		5/1988	Robinson et al.			
		A44	4	9	4	2	5	5	6		7/1990	Sasaki et al.			
		A45	4	4	0	5	9	5	2		9/1983	Slakmon			
		A46	4	6	7	2	2	4	0		6/1987	Smith et al.			
		A47	4	2	5	0	5	7	0		2/1981	Tsang et al.			
		A48	4	6	0	1	0	3	1		7/1986	Walker et al.			
		A49	4	2	8	1	3	9	8		7/1981	McKenny et al.			
↓		A50	4	6	1	7	6	5	1		10/1986	Ip, et al.			

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		DOCUMENT NUMBER									DATE	COUNTRY	CLASS	SUB CLASS	TRANS. (YES/NO)
Pme		B16	WO	8	4	0	0	6	2	8	2/1984	PCT W.I.P.O.			
		B17	AO	1	0	5	4	5	4	3	3/1989	Japanese Patent Abstr.			Yes
↓		B18	A6	0	1	7	8	5	6	4	2/1986	Japanese Patent Abstr.			Yes

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

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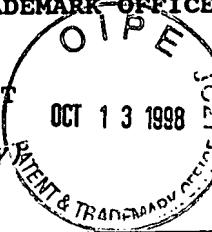
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*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
PMC	A51	4 4 4 9 2 0 5	5/ 1984	Hoffman			
	A52	4 8 0 5 1 0 9	2/ 1989	Kroll et al.			
	A53	4 8 2 1 2 4 0	4/ 1989	Nakamura et al.			
	A54	4 8 8 2 6 4 2	11/ 1989	Tayler et al.			
	A55	4 9 2 0 4 7 8	4/ 1990	Furuya et al.			
	A56	4 9 3 3 9 0 6	6/ 1990	Terada et al.			
	A57	5 1 3 6 5 4 6	8/ 1992	Fukuda et al			
	A58	5 0 5 1 8 8 7	9/ 1991	Berger et al.			
	A59	4 9 1 6 6 0 5	4/ 1990	Beardsley et al.			
	A60	4 4 6 6 0 5 9	8/ 1984	Bastian et al.			
	A61	5 0 4 3 9 4 0	8/ 1991	Harari			
	A62	5 1 7 2 3 3 8	12/ 1992	Mehrotra et al.			
	A63	5 6 7 1 2 2 9	9/ 1997	Harari et al.			
	A64	5 2 9 7 1 4 8	3/ 1994	Harari et al.			
	A65	5 3 5 9 5 6 9	10/ 1994	Fujita et al.			
	A66	5 4 3 0 8 5 9	7/ 1995	Norman et al.			
	A67	5 4 8 8 7 1 1	1/ 1996	Hewitt et al.			
	A68	5 6 0 6 5 3 2	2/ 1997	Lambrache et al.			
	A69	5 5 4 6 3 5 1	8/ 1996	Tanaka et al.			

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		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS. (YES/1)

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

PMC	C11	Bleiker et al., "A Four-State EEPROM Using Floating-Gate Memory Cells," IEEE Journal of Solid-State Circuits, SC-22 (1987) June, No. 3, New York, NY, USA
PMC	C12	Intel Corporation, 27F256, 256K (32K x 8) CMOS FLASH MEMORY, May 1988, pp. 1-21

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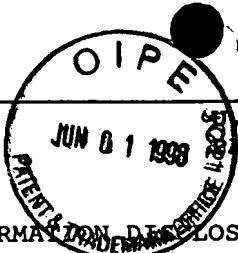
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS (YES/
<i>pme</i>	C13	Krick, "Three-State MNOS FET Memory Array," <u>IBM Technical Disclosure Bulletin</u> , Vol. 18, No. 12, May 1976, pp. 4192-4193					
	C14	Alberts C.S. et al., "Multi-Bit Storage FET EAROM Cell," <u>IBM Technical Disclosure Bulletin</u> , Vol. 24, No. 74, December 1981, pp 3311-3314					
	C15	Horiguchi et al., "An Experimental Large-Capacity Semiconductor File Memory Using 16-Levels Cell Storage," <u>IEEE Journal of Solid-State Circuits</u> , Vol. 23, No. 1, February 1988, pp.27-33					
	C16	Furuyama, et al., "An Experimental 2-Bit/Cell Storage Dram for Macro Cell or Memory-on-logic Application," <u>1988 IEEE</u> , pp. 4.4.1 to 4.4.4					
<i>✓</i>	C17	Stark, "Two Bits Per Cell ROM," <u>1981 IEEE Catalog No. 81-CH1626-1</u> , pp. 201-212					

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*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
A1	4 0 9 3 9 8 5	1978	Das			
A2	4 2 7 9 0 2 4	1981	Schrenk			
A3	4 6 1 6 3 1 1	1986	Sato			
A4	4 7 1 8 0 4 1	1988	Baglee et al.			
A5	4 7 8 5 4 2 5	1988	Lavelle			
A6	4 8 0 0 5 2 0	1989	Iijima			98
A7	4 8 8 7 2 3 4	1989	Iijima			JUN 10
A8	4 9 4 9 2 4 0	1990	Iijima			11
A9	5 0 5 3 9 9 0	1991	Kreifels et al.			12
A10	5 0 7 0 4 7 4	1991	Tuma et al.			13
A11	5 0 9 5 3 4 4	1992	Harari			14

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	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
B1	58 - 2 1 5 7 9 4	1983	Japan			Yes
B2	58 - 2 1 5 7 9 5	1983	Japan			Yes
B3	59 - 1 6 2 6 9 5	1984	Japan			Yes
B4	60 - 2 1 2 9 0 0	1985	Japan			Yes
B5	62 - 2 8 3 4 9 6	1987	Japan			Yes

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

C1	Lucero et al., "A 16 kbit Smart 5 V-only EEPROM with Redundancy," <i>IEEE Journal of Solid-State Circuits</i> , vol. SC-18, no. 5, pps. 539-543 (October 1983)
C2	Torelli et al., "An improved method for programming a word-erasable EEPROM," <i>Alta Frequenza</i> , vol. 52, no. 6, pps. 487-494 (Nov.-Dec. 1983)
C3	Data Sheet: "27F256 256K(32K x 8) CMOS Flash Memory," Intel Corporation, pps. 1-24 (May 1988)

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## U. S. PATENT DOCUMENTS

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	A12 5 2 2 6 1 6 8	1993	Kobayashi et al.			
	A13 4 2 1 0 9 5 9	1980	Wozniak			
	A14 4 6 4 2 7 5 9	1987	Foster			
	A15 4 4 5 6 9 7 1	1984	Fukuda et al.			
	A16 4 2 9 5 2 0 5	1981	Kunstadt			
	A17 4 6 1 7 6 2 4	1986	Goodman			
	A18 4 3 5 4 2 5 3	1982	Naden			
	A19 4 4 2 2 1 6 1	1983	Kressel et al.			
	A20 4 4 5 0 5 5 9	1984	Bond et al.			
	A21 4 6 5 4 8 4 7	1987	Dutton			
	A22 4 7 3 3 3 9 4	1988	Burkhard			

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	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
	B6 60 - 0 7 6 0 9 7	1985	Japan			Abstr
	B7 59 - 4 5 6 9 5	1984	Japan			Abstr
	B8 61 - 9 6 5 9 8	1986	Japan			Abstr
	B9 62 - 2 8 3 4 9 7	1987	Japan			Abstr
	B10 63 - 1 8 3 7 0 0	1988	Japan			Abstr

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

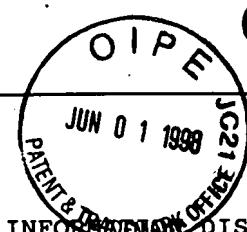
C4	Preliminary Data Sheet, "48F512 512K Flash EEPROM," SEEQ Technology, Incorporated, pps. 2-1 thru 2-12 (October 1988)
C5	Advanced Data Sheet, "48F010 1024K Flash EEPROM," SEEQ Technology, Incorporated, pps. 2-13 thru 2-24 (October 1988)
C6	Lai, Robert S., Writing MS-DOS Device Drivers, The Waite Group, Inc., September 1987, pp. i-xi and 235-319

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*EXAMINER INITIAL		DOCUMENT NUMBER							DATE	NAME	CLASS	SUB CLASS	FILING DATE
	A23	4	8	9	6	2	6	2	1990	Wayama et al.			
	A24	4	9	4	5	5	3	5	1990	Hosotani et al.			
	A25	4	3	8	0	0	6	6	1983	Spencer et al.			
	A26	4	4	6	3	4	5	0	1984	Haeusele	98		
	A27	4	3	5	5	3	7	6	1982	Gould	RECEIVED	10/14/97	AMID: 014
	A28	3	6	3	3	1	7	5	1972	Harper	RECEIVED	10/14/97	AMID: 014
	A29	4	4	9	8	1	4	6	1985	Martinez	RECEIVED	10/14/97	AMID: 014
	A30	4	9	2	4	3	3	1	1990	Robinson et al.	RECEIVED	10/14/97	AMID: 014
	A31	4	4	7	9	2	1	4	1984	Ryan	RECEIVED	10/14/97	AMID: 014
	A32	4	9	5	3	1	2	2	1990	Williams	RECEIVED	10/14/97	AMID: 014
	A33	4	9	2	0	5	1	8	1990	Nakamura et al.	RECEIVED	10/14/97	AMID: 014

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	B11	0	0	8	6	8	8	6	1983	European Patent Appln.			
	B12	2	1	3	6	9	9	2	1984	UK Patent Appln.			
	B13	0	2	4	3	5	0	3	1987	European Patent Appln.			
	B14	0	3	0	0	2	6	4	1989	European Patent Appln.			
	B15	0	5	5	7	7	2	3	1987	AU Patent Abridgement			

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

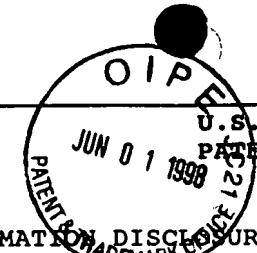
	C7	Miller, "Semidisk Disk Emulator," <i>Interface Age</i> , p. 102, November, 1982
	C8	Clewitt, "Bubble Memories as a Floppy Disk Replacement," <i>1978 MIDCON Technical Papers</i> , vol. 2, pp. 1-7, Dec. 1978
	C9	Hancock, "Architecting a CCD Replacement for the IBM 2305 Fixed Head Disk Drive," <i>Digest of Papers, Eighteenth IEEE Computer Society International Conference</i> , pp. 182-184, 1979
	C10	Wilson, "1-Mbit flash memories seek their role in system design," <i>Computer Design</i> , vol. 28, no. 5, pps. 30-32 (March 1989)

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	A36	4	9	1	4	5	2	9		1990	Bonke			
	A37	4	0	5	1	3	5	4		1977	Choate			
	A38	5	1	6	3	0	2	1		1992	Mehrotra et al.			
	A39	4	5	1	4	8	3	0		1985	Hagiwara et al.			
	A40	4	7	9	4	5	6	8		1988	Lim et al.			
	A41	4	6	1	2	6	4	0		1986	Mehrotra et al.			
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	A43	4	7	4	6	9	9	8		1988	Robinson et al.			
	A44	4	9	4	2	5	5	6		1990	Sasaki et al.			
	A45	4	4	0	5	9	5	2		1983	Slakmon			
	A46	4	6	7	2	2	4	0		1987	Smith et al.			
	A47	4	2	5	0	5	7	0		1981	Tsang et al.			
	A48	4	6	0	1	0	3	1		1986	Walker et al.			
	A49	4	2	8	1	3	9	8		1981	McKenny et al.			
	A50	4	6	1	7	6	5	1		1986	Ip, et al.			

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	B17	AO	1	0	5	4	5	4	3	1989	Japanese Patent Abstr.			Yes
	B18	A6	0	1	7	8	5	6	4	1986	Japanese Patent Abstr.			Yes

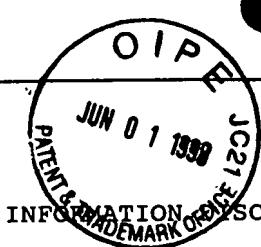
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	A52	4 8 0 5 1 0 9	1989	Kroll et al.			
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	A55	4 9 2 0 4 7 8	1990	Furuya et al.			
	A56	4 9 3 3 9 0 6	1990	Terada et al.			
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	A61	5 0 4 3 9 4 0	1991	Harari			
	A62	5 1 7 2 3 3 8	1992	Mehrotra et al.			
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	A65	5 3 5 9 5 6 9	1994	Fujita et al.			
	A66	5 4 3 0 8 5 9	1995	Norman et al.			
	A67	5 4 8 8 7 1 1	1996	Hewitt et al.			
	A68	5 6 0 6 5 3 2	1997	Lambrache et al.			
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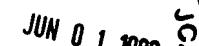
	C11	Bleiker et al., "A Four-State EEPROM Using Floating-Gate Memory Cells," <u>IEEE Journal of Solid-State Circuits</u> , SC-22 (1987) June, No. 3, New York, NY, USA
	C12	Intel Corporation, 27F256, 256K (32K x 8) CMOS FLASH MEMORY, May 1988, pp. 1-21

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		FILED September 16, 1997	GROUP 2785

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	C14	Alberts C.S. et al., "Multi-Bit Storage FET EAROM Cell," <u>IBM Technical Disclosure Bulletin</u> , Vol. 24, No. 74, December 1981, pp 3311-3314					
	C15	Horiguchi et al., "An Experimental Large-Capacity Semiconductor File Memory Using 16-Levels Cell Storage," <u>IEEE Journal of Solid-State Circuits</u> , Vol. 23, No. 1, February 1988, pp.27-33					
	C16	Furuyama, et al., "An Experimental 2-Bit/Cell Storage Dram for Macro Cell or Memory-on-logic Application," <u>1988 IEEE</u> , pp. 4.4.1 to 4.4.4					
	C17	Stark, "Two Bits Per Cell ROM," <u>1981 IEEE Catalog No. 81-CH1626-1</u> , pp. 201-212					

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